FET Inrush Protection

Chris Pavlina
https://semianalog.com

2015-11-23

Abstract

It is possible to use a simple one-transistor FET circuit to provide inrush protection for low voltage DC circuits. With the addition of only one more FET, reverse-polarity protection can also be provided. Suggested applications include USB devices (as the USB specification is strict about inrush) and anything requiring significant bulk decoupling.

TL;DR: If you don't care how this circuit works, feel free to skip to section 6 (Design equations) and section 7 (Gotchas).

Contents

1 What not to do

There is a circuit that is occasionally seen[4], that adds a single capacitor onto the familiar MOS reverse-polarity protection circuit:

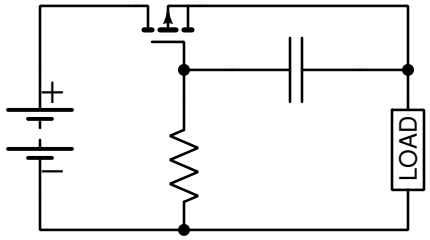

Figure 1: Don't do this!

It should be fairly obvious why this won't work. The mechanism of the reverse-polarity circuit is that the body diode conducts until the load is *almost* fully powered, and then the voltage at the load provides enough V_{GS} bias to the FET to turn it on completely. There is nothing we can do to control the behavior of the body diode, so clearly nothing can be built onto this circuit to slow the current.

Flipping the FET around so the body diode is no longer in circuit (losing the reverse protection behavior) won't work either! The FET has very high voltage gain, so using an RC circuit to ramp its gate voltage won't do much. The output voltage will still spike up quickly, allowing a large inrush. This just *delays* startup.

2 Better, but not quite

What is needed is something a bit more clever:

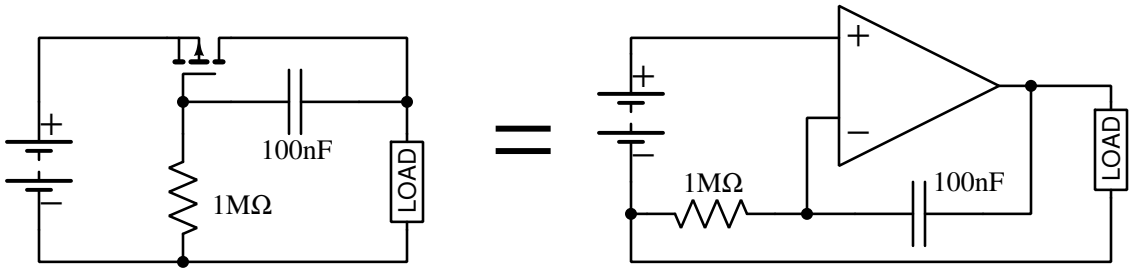

Figure 2: More clever, but still don't do it!

Imagining the FET as a differential amplifier, we can see that the circuit is actually an integrator. When the input power is connected, the waveform seen at the input is a step, and the integral of a step is a ramp — perfect! If we can control the slope of that ramp, we can easily control the inrush into our circuit's capacitance.

3 Debugging

Let's build and test the circuit, with a 12 V source and a 1000 µF capacitor as a load. The inrush current of this circuit, as will be seen later in the design equations, should be on the order of 120 mA.

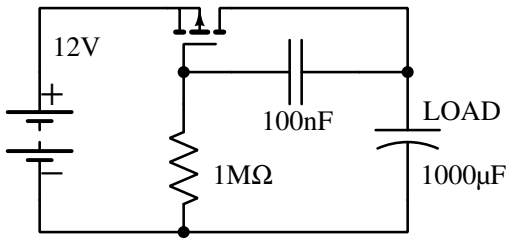

Figure 3: The circuit we're going to test.

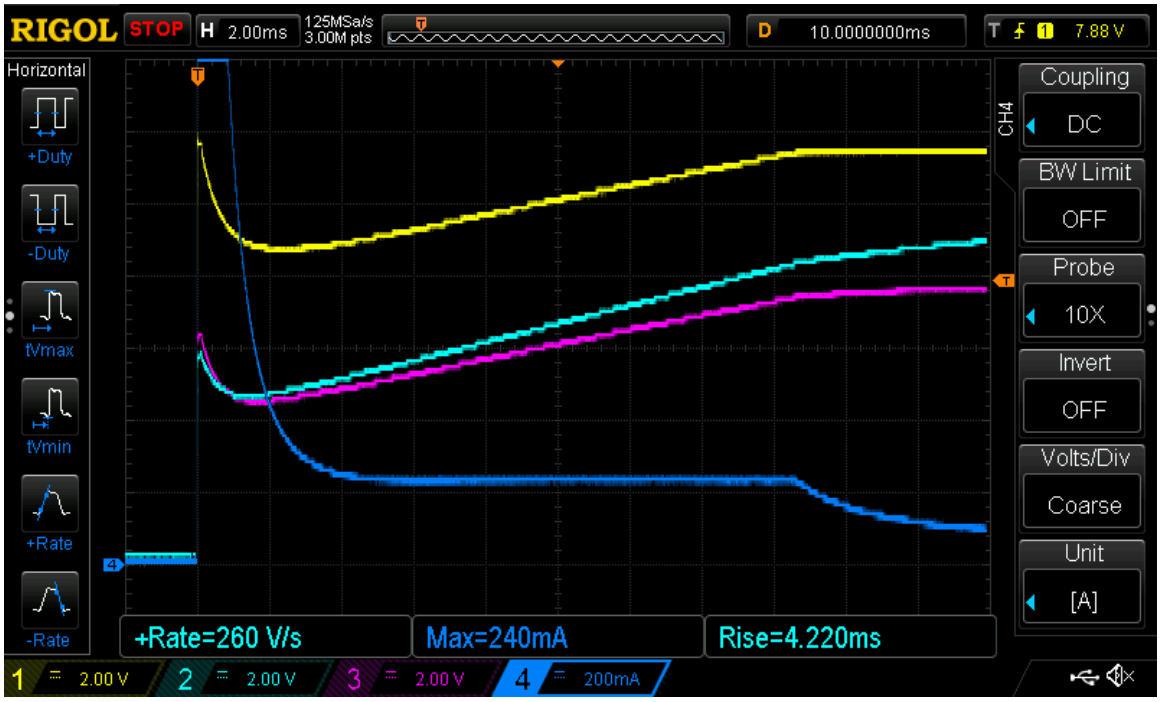

Figure 4: Test of faulty circuit. Channels: 1 = input, 2 = output, 3 = gate voltage, 4 = inrush current

The inrush current spikes very high, saturating the oscilloscope at well over 1.4 A for about 1 ms, and sits at about 200 mA for about 14 ms until it tails off. The problem is that the FET only behaves as an integrator when it is in its linear region of operation. The 100 nF timing capacitor holds the gate to the drain as the input voltage is stepped, and the source quickly rises high enough for this to put it in saturation.

Theoretically, any number of components can be added between the input node of an integrator and a fixed voltage without changing the behavior of the integrator. Taking advantage of this, we'll add a much larger capacitor between the FET's gate and source to swamp this effect.

4 The working circuit

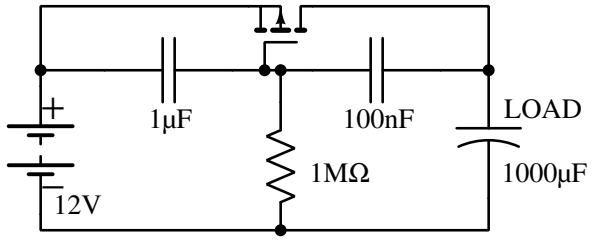

Figure 5: A second capacitor is added to prevent immediate saturation.

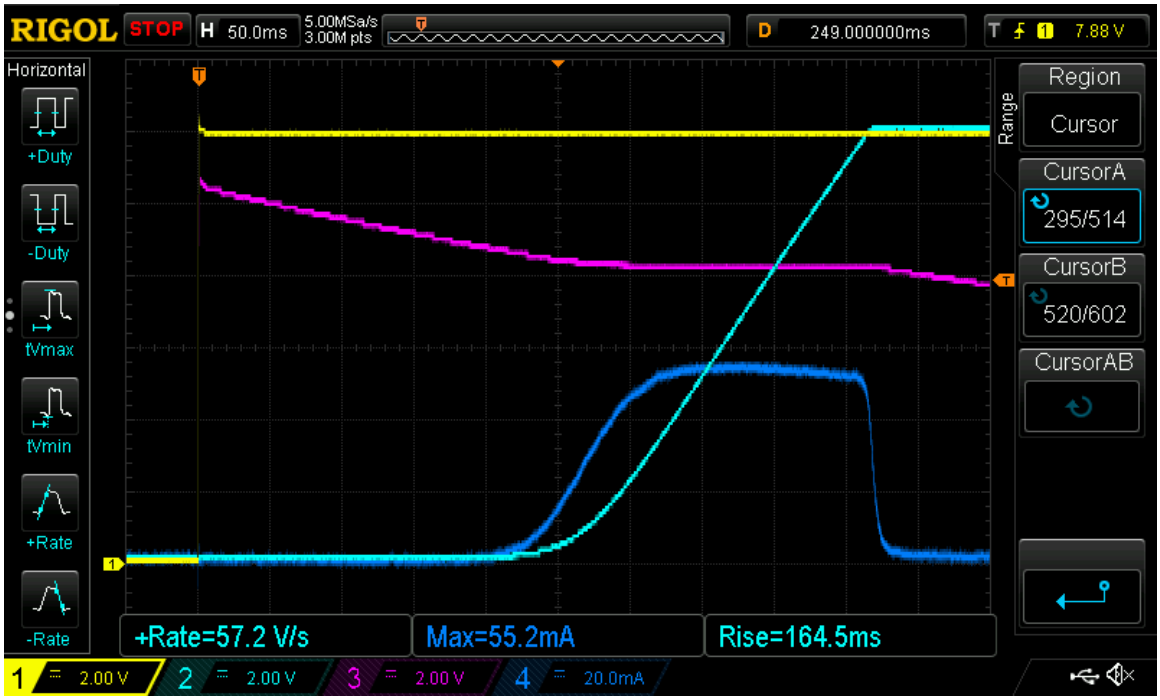

Figure 6: Test of good circuit. Channels: 1 = input, 2 = output, 3 = gate voltage, 4 = inrush current

This one works! The additional capacitor delays startup by about 250 ms, at which point V_{GS} reaches the threshold point and the FET begins to integrate the voltage step. The voltage rises at about 57 V/s, giving an inrush current of at most about 55 mA.

5 Deriving the design equations

The circuit is essentially just an integrator:

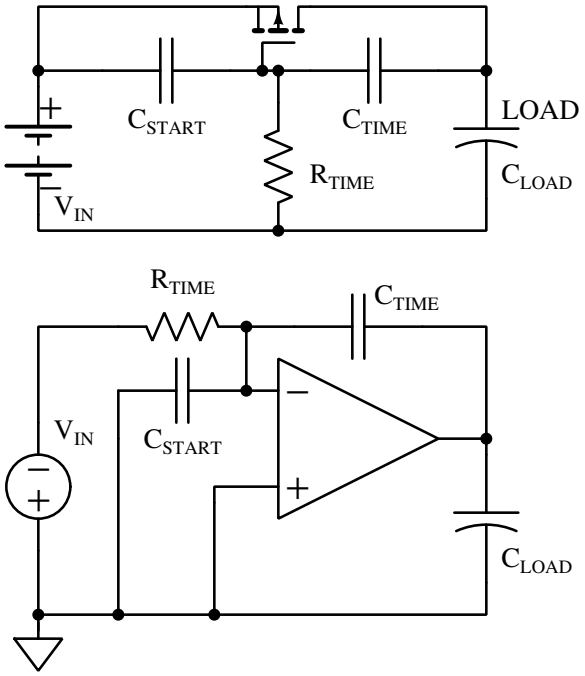

Figure 7: The full circuit and its equivalent integrator.

Note that the equivalent integrator circuit "sees" the input step as the *negative* of the input voltage. This is because the noninverting input (the FET's source) sits at the positive rail, and the timing resistor runs to the negative rail.

The behavior of an integrator is[1, p. 230]:

$$V_{out}(t) = \frac{-1}{R \cdot C} \int V_{in}(t)\ dt + \text{const}$$

For a stepped input voltage, we can rearrange this to get the slope of the output:

$$\frac{d}{dt} V_{out}(t) = \frac{-1}{R \cdot C} V_{in}(t)$$

In the ideal integrator circuit above, the voltage across C_{START} will be zero at all times, so it can be ignored. Therefore, the slope of the output voltage will be:

$$\frac{d}{dt} V_{out}(t) = \frac{V_{IN}}{R_{TIME} \cdot C_{TIME}}$$

A capacitor behaves according to $i = C \cdot \frac{d}{dt} v$ [1, p. 19], so we can find the current into the capacitor:

$$I = C_{LOAD} \cdot \frac{d}{dt} V_{OUT} = \frac{C_{LOAD} \cdot V_{IN}}{R_{TIME} \cdot C_{TIME}}$$

The ramp time will be equal to the input voltage divided by the slope:

$$t_{RAMP} = \frac{V_{IN}}{\frac{d}{dt} V_{OUT}}$$

We must compute the power dissipation in the FET to select an appropriate one. The instantaneous power dissipation is:

$$p(t) = (v_{out} - v_{in}) \cdot i_{out}$$

The average over the pulse is:

$$P = \frac{1}{t_{RAMP}} \int ((v_{out} - v_{in}) \cdot i_{out})\, dt$$

i_{out} is constant, and $v_{out} - v_{in}$ is a linear slope, making the area under this curve triangular. The integral can be computed geometrically:

$$A_{triangle} = \frac{1}{2}(w \cdot h)$$

$$P = \frac{1}{t_{RAMP}} \cdot \frac{1}{2} (V_{IN} \cdot t_{RAMP} \cdot I_{OUT})$$

$$P = \frac{1}{2} (V_{IN} \cdot I_{OUT})$$

Now, we must derive C_{START}. At inrush, C_{START} and C_{TIME} behave as a capacitive voltage divider, and these must keep V_{GS} between zero and the threshold voltage at all times.

$$V_{GS} = V_{IN} \cdot \frac{C_{TIME}}{C_{TIME} + C_{START}}$$

$$C_{START} = C_{TIME} \cdot \left(\frac{V_{IN}}{V_{GS(th)}} - 1 \right)$$

This equation describes the critical case, so for error margin we want:

$$C_{START} > C_{TIME} \cdot \left(\frac{V_{IN}}{V_{GS(th)}} - 1 \right)$$

6 Design equations

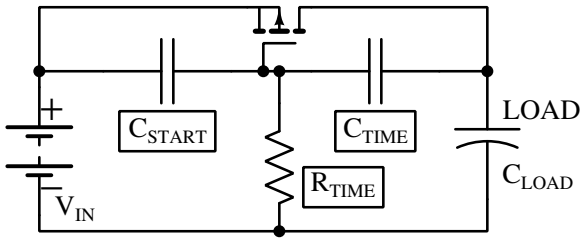

Figure 8: The full circuit with parts labeled. Unknowns are in boxes.

1. The input voltage V_{IN} and the load capacitance C_{LOAD} are known as part of your application.

2. Determine I_{INR}, the desired inrush current.

3. Compute the resulting output voltage slope, $\frac{d}{dt}V_{OUT}$:

$$\frac{d}{dt}V_{OUT} = \frac{I_{INR}}{C_{LOAD}}$$

4. Select R_{TIME} and C_{TIME}. Note that either one of them can be freely chosen, and the other one computed:

$$R_{TIME} \cdot C_{TIME} = \frac{V_{IN}}{\frac{d}{dt}V_{OUT}}$$

5. Compute the power dissipation and ramp time:

$$P = \frac{1}{2}\left(V_{IN} I_{IN}\right)$$
$$t_{RAMP} = \frac{V_{IN}}{\frac{d}{dt}V_{OUT}} = R_{TIME} \cdot C_{TIME}$$

6. Select a MOSFET. Ensure that its V_{DS} rating can handle the supply voltage, its $R_{DS(on)}$ is low enough for your application, and that its FBSOA (forward-bias safe operating area) allows for a pulse of the above computed amplitude and duration. Note its minimum $V_{GS(th)}$ for the next part.

7. Compute C_{START}. For error margin, it should be at least double the computed value, but do not make it *too* big, or the startup delay will be unnecessarily long:

$$C_{START} > C_{TIME} \cdot \left(\frac{V_{IN}}{V_{GS(th)}}\right)$$

7 Gotchas

This circuit isn't perfect. There are few traps and drawbacks:

- As presented, the MOSFET must have a $V_{GS(max)}$ rating in excess of V_{IN}. If this is impractical, a second resistor R_{LIMIT} can be placed in parallel with C_{START}, forming a voltage divider to set the final gate voltage.

  Perhaps counter-intuitively, this does not change the timing resistance to be the Thévenin equivalent of R_{LIMIT} and R_{TIME}, for the same reason that C_{START} does not affect the timing.

- This circuit only limits capacitive inrush. If your inrush is for other reasons, for instance V_{DD} ramp inrush of a large digital device like an FPGA, it may actually worsen it. Mind the maximum ramp times of the devices you are powering. If you have voltage regulators downstream, it may be desirable to add an RC delay to their enable inputs to start them after this circuit has stabilized.

- This is not a precision circuit! For the example above, I_{INR} should have been $\frac{C_{LOAD} \cdot V_{IN}}{R_{TIME} \cdot C_{TIME}} = \frac{1000\,\mu F \cdot 12\,V}{1\,M\Omega \cdot 100\,nF} = 120\,mA$, but it was actually 55 mA, a massive -54% error! Note that SPICE simulation verifies the accuracy of these equations, so other real-world effects were at play here. When using more ideal components (accurate ceramic capacitors with low $C(V)$ dependence, in particular), the real measurements will be closer to the predicted values.
- This circuit does not provide reverse-polarity protection. It can be modified with one additional FET, though — dual MOSFETs with both devices in the same package are handy here:

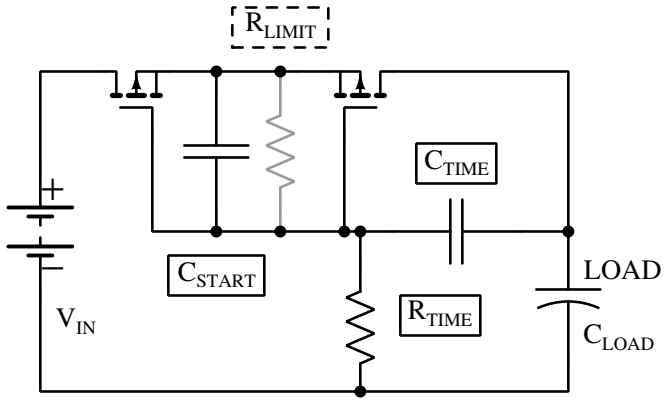

Figure 9: The full circuit with additional RPP.

8 Worked example

As an example, we'll design an inrush limiter for a USB device. Specifications are:

- V_{IN}: 5 V nominal
- C_{LOAD}: 220 µF
- I_{OUT} at startup: 20 mA
- Maximum I_{IN}: 113 mA [3]
- C_{IN}: min. 1 µF, max. 10 µF [3]

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1. The input voltage V_{IN} and the load capacitance C_{LOAD} are known as part of the application.
2. I_{IN} must not exceed 113 mA, and the load will draw $I_{OUT} = 20\,mA$ at startup, so I_{INR} must not exceed $113\,mA - 20\,mA = \boxed{93\,mA}$.

3. Compute the resulting output voltage slope, $\frac{d}{dt}V_{OUT}$:

$$\frac{d}{dt}V_{OUT} = \frac{I_{INR}}{C_{LOAD}}$$
$$\frac{d}{dt}V_{OUT} = \frac{93\,mA}{220\,\mu F} = \boxed{423\,V/s}$$

4. Select R_{TIME} and C_{TIME}. It is likely that the system will already contain 100 nF capacitors, so we'll set $C_{TIME} = \boxed{100\,nF}$.

$$R_{TIME} \cdot C_{TIME} = \frac{V_{IN}}{\frac{d}{dt}V_{OUT}}$$
$$R_{TIME} = \frac{V_{IN}}{C_{TIME} \cdot \frac{d}{dt}V_{OUT}} = 118\,k\Omega \approx \boxed{120\,k\Omega}$$

5. Compute the power dissipation and ramp time. Note that this uses I_{IN}, the total input current, not I_{INR}, the inrush current to the capacitor.

$$P = \frac{1}{2}\left(V_{IN} I_{IN}\right)$$
$$P = \frac{1}{2}\left(5\,V \cdot 113\,mA\right) = \boxed{283\,mW}$$

$$t_{RAMP} = \frac{V_{IN}}{\frac{d}{dt}V_{OUT}} = R_{TIME} \cdot C_{TIME}$$
$$t_{RAMP} = (120\,k\Omega) \cdot (100\,nF) = \boxed{12\,ms}$$

6. Select a MOSFET. I'm going to use International Rectifier's IRLML6402, which has a low $R_{DS(on)}$ of 65 mΩ, a minimum $V_{GS(th)}$ of 400 mV, and fits the above power dissipation nicely into its FBSOA[2].

7. Compute C_{START}. For error margin, it should be at least double the computed value, but do not make it *too* big, or the startup delay will be unnecessarily long:

$$C_{START} > C_{TIME} \cdot \left(\frac{V_{IN}}{V_{GS(th)}}\right)$$
$$C_{START} > (100\,nF) \cdot \left(\frac{5\,V}{0.4\,V}\right)$$
$$C_{START} > \boxed{1.25\,\mu F}$$

   A 2.2 µF capacitor would be reasonable for C_{START} and give some error margin.

8. The USB example is unique in that it has a *minimum* input capacitance, of 1 µF. The input capacitance of this circuit itself is the series combination of C_{START}, C_{TIME}, and C_{LOAD}, which is 96 nF. We'll add a second 2.2 µF at the input, which places the total input capacitance at about 2.3 µF.

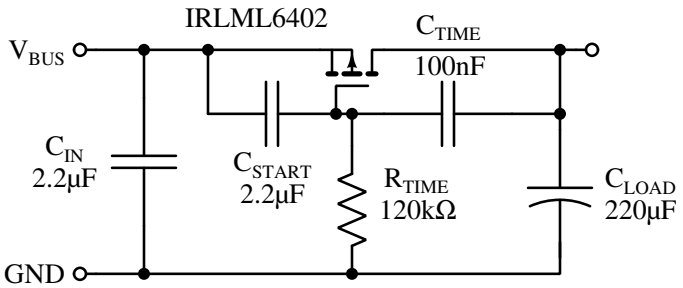

Figure 10: Example with values

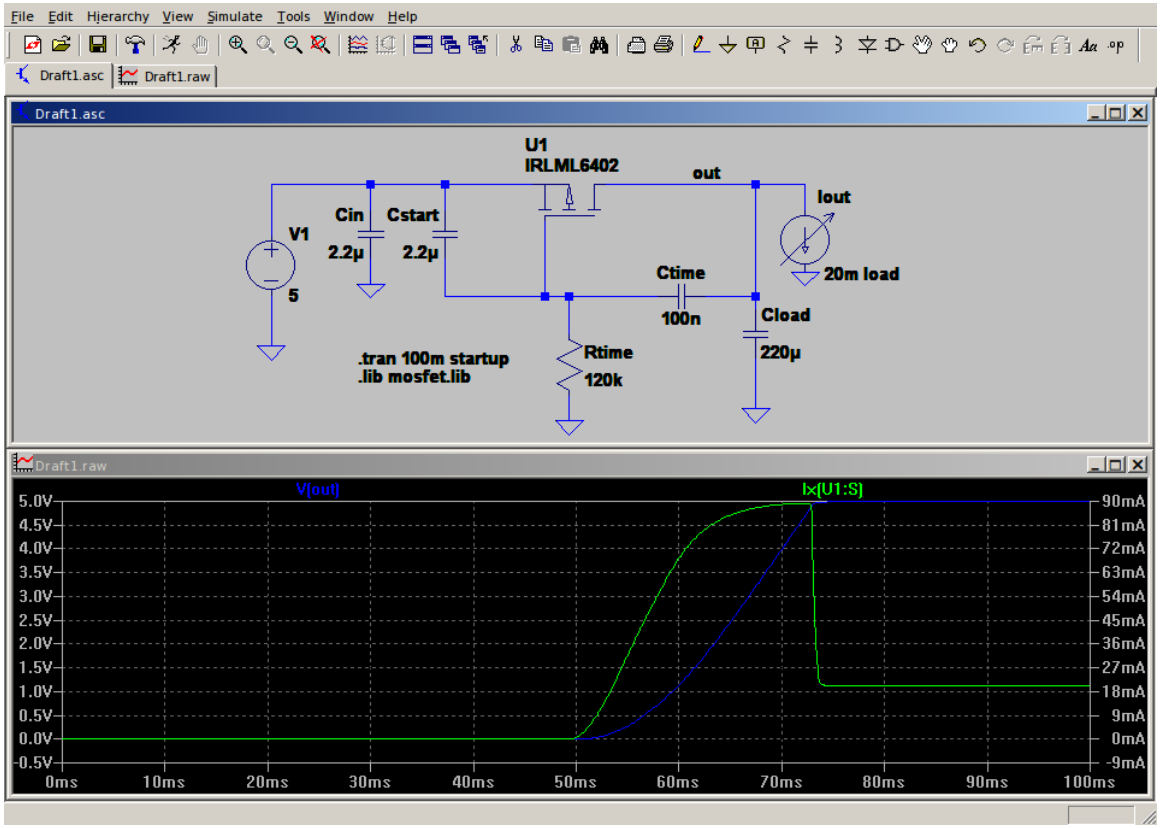

Figure 11: Simulated example

References

[1] P. Horowitz and W. Hill, The art of electronics, 3rd ed. Cambridge [England]: Cambridge University Press, 2014.

[2] International Rectifier, IRLML6402PbF HEXFET® Power MOSFET, 2014. [Online]. Available: http://www.irf.com/product-info/datasheets/data/irlml6402pbf.pdf. [Accessed: 23 Nov 2015].

[3] USB Implementers Forum, Universal Serial Bus Specification, rev 2.0. 2000, pp. 7.2.4.1. Available: http://www.usb.org/developers/docs/usb20_docs/.

[4] J. Walker, 'FET Supplies Low-Voltage Reverse-Polarity Protection', ElectronicDesign.com, 2005. [Online]. Available: http://electronicdesign.com/power/fet-supplies-low-voltage-reverse-polarity-protection. [Accessed: 23 Nov 2015].